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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,053	11/18/2003	Bruce G. Hazelzet	BUR920020085US1	1052

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IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
1000 RIVER STREET
972 E
ESSEX JUNCTION, VT 05452

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,053	HAZELZET ET AL.	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-10 and 12-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6,8-10 and 12-16* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated July 27, 2007, claims 1, 2, 4, 6-10 and 12-16 are active in this application.

In view of newly found art, the indication for allowability in the prior office action has been withdrawn.

Specification

2. If there are cross-reference to related applications, please include the respective patent numbers, if known.

Claim Objections

3. Claims 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections- 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claim 16 is rejected under 35 U.S.C 102(b) as being anticipated by Morishima [U.S. Patent Application #20020064075].

With respect to claim 16, Morishima disclose, in figures 1-3, a computer system with a memory system comprising: memory devices and re-drive circuitry [3] external to the said memory devices, said re-drive circuitry adapted to invert an address [YO] or

command input signal subsequently output to one or more of the plurality of DRAMs [MA's] via a programmable input [input electrodes], such that simultaneous switching noise is reduced inverted signals based on a selected operation mode [inherent – see Summary of Invention, paragraph 0047].

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 4 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dell et al. [U.S. Patent # 5,513,135] in view of Itou [U.S. Patent # 5,999,483].

Dell et al. disclose a memory system comprising: a plurality of DRAMs [see specification – it is noted that Dell et al. also stated that DRAMs and SDRAMs are interchangeable].

Itou discloses all of the above mentioned but is silent about the internal elements of the SDRAM device. However, this is not new. Itou disclose sDRAMs having circuits to accept non-inverted input signals and inverted input signals [see figure 2]; a register programmed [13] to provide inverted or non-inverted signals to the sDRAMS; and programmable pins in the register and the sDRAMs to enable operation in either non-inverted or inverted mode, wherein one programmable pin is connected to ground to provide one mode and the other programmable pin is connected to Vdd to operate in the other mode [it is interpreted that the pins are programmable since they are able to receive the applied signals whenever they are active]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dell et al. memory circuit element to include the element as taught by Itou, since the modification is merely a substitution of a functionally recognized equivalent element.

With respect to claim 2, Itou disclose, in figure 2, re-drive circuitry [output of one inverter and input to another inverter], which can output both non-inverted and inverted polarity signals from one or more input signals.

With respect to claim 4, Dell et al. disclose the DRAMs are mounted on a DIMM. See specification.

With respect to claim 9, Itou disclose, in figure 2, the register drives either non-inverted or inverted signals to the DRAMs using a programmable pin.

8. Claims 6 and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dell et al. [U.S. Patent # 5,513,135] in view of Itou [U.S. Patent # 5,999,483].

Dell et al. disclose a memory system comprising: a plurality of DRAMs [see specification – it is noted that Dell et al. also stated that DRAMs and SDRAMs are interchangeable].

Itou discloses all of the above mentioned but is silent about the internal elements of the SDRAM device. However, this is not new. Itou disclose receiver circuits [see figure 2] adapted to interface with a plurality of signal drivers capable of providing both non-inverted and inverted address and command signal polarities to the plurality of sDRAMs; a memory controller [see figures 1 and 2] which is capable of configuring the plurality of DRAMs to accept either non-inverted or inverted signals using a programmable pin [it is interpreted that the pins are programmable since they are able Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dell et al. memory circuit element to include the element as taught by Itou, since the modification is merely a substitution of a functionally recognized equivalent element.

With respect to claim 8, both Dell et al. and Itou disclose the pin is hard-wired to the DRAMs. See figures.

9. Claims 10 and 12-14 are rejected under 35 U.S.C. § 103(a) as being

unpatentable over Dell et al. [U.S. Patent # 5,513,135] in view of Itou [U.S. Patent # 5,999,483].

Dell et al. disclose a memory system comprising: a module having plurality of DRAMs [see specification – it is noted that Dell et al. also stated that DRAMs and SDRAMs are interchangeable].

Itou discloses all of the above mentioned but is silent about the internal elements of the SDRAM device. However, this is not new. Itou disclose DRAMs with inputs and outputs and circuits to accept either non-inverted input signals and inverted input signals [see figure 2], wherein pre-selected DRAMs may operate in the inverted mode with some critical signals remaining in a non-inverted mode; a means [131] connected to the circuits for changing modes to accept inverted input signals; and a memory controller [16 or see figure 1] which is programmable to operate in non-inverted mode at power up and to change after it is programmed. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dell et al. memory circuit element to include the element as taught by Itou, since the modification is merely a substitution of a functionally recognized equivalent element.

With respect to claim 12, Itou disclose, in figure 2, the memory controller may operate in the inverted mode with some critical signals remaining in non-inverted mode. See specification.

With respect to claim 13, Dell et al. disclose a programmable pin is hard-wired to the module. See figures.

With respect to claim 14, Itou disclose, in figure 2, the means for changing modes includes a pin that is controlled by the memory controller. See specification.

10. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dell et al. [U.S. Patent # 5,513,135] in view of Itou [U.S. Patent # 5,999,483].

Dell et al. disclose DIMM comprising: a module having plurality of DRAMs [see specification – it is noted that Dell et al. also stated that DRAMs and SDRAMs are interchangeable].

Itou discloses all of the above mentioned but is silent about the internal elements of the SDRAM device. However, this is not new. Itou disclose DRAMs with means for operating with non-inverted or inverted signals based on a pre-selected operating mode [see figure 2]; and signal re-drive circuitry [output of one inverter inputting to another inverter] adapted to invert an address or command input signal subsequently output to one or more of the plurality of DRAMs, wherein an output mode of the signal re-drive circuitry is responsive to a programmable input [controller]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dell et al. memory circuit element to include the element as taught by Itou, since the modification is merely a substitution of a functionally recognized equivalent element.

Allowable Subject Matter

11. The following is an Examiner's statement of reasons for the indication of

allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- the memory controller dynamically configures polarities of address and command signals exchanged between a plurality of signal drivers and the plurality of DRAMs, such that simultaneous switching noise is reduced in the memory system.

Conclusion

12. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

13. .Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

14. .Any inquiry of a general nature or relating to the status of this application. should be directed to the Group receptionist whose telephone number is (571) 272-1650.

/Michael T. Tran/
Michael T. Tran
Art Unit 2827
October 14, 2008